QUANTUM DOT VERTICAL CAVITY SURFACE EMITTING LASER

Inventors: Xiaodong Huang, Andreas Stintz, Kevin Malloy, Guangtian Liu, Luke Lester, and Julian Cheng

STATEMENT AS TO FEDERALLY SPONSORED RESEARCH AND DEVELOPMENT

[0001] The U.S. Government may have certain rights in this invention pursuant to research conducted under the following grants: Grant No. F49620-95-1-0530 awarded by the Air Force Office Of Science and Research, Grant No. DAAL01-96-02-0001 awarded by the Army Research Lab, Grant No. F4920-99-1-330 awarded by the Air Force Office of Science and Research, and Grant No. MDA972-98-1-0002 awarded by the Defense Advanced Research Projects Agency.

RELATED APPLICATIONS

[0002] This application claims priority under 35 U.S.C.§ 119(e) to the following United States Patent Application Nos.: 60/276,186, entitled "Semiconductor Quantum Dot Laser Active Regions Based On Quantum Dots in

a Optimized Strained Quantum Well," filed March 16, 2001; 60/272,307, entitled "Techniques for Using Quantum Dot Active Regions In Vertical Cavity Surface Emitting Lasers," filed March 2, 2001; 60/316,305, entitled "Quantum Dot And Quantum Dash Active Region Devices," filed August 31, 2001. The contents of all of the above applications are hereby each incorporated by reference in their entirety in the present patent application.

[0003] This application is also related to U.S. Pat. App. Ser. No. 09/972,303 "Quantum Dot Lasers," on October 5, 2001, commonly owned by the assignee of the present patent application, the contents of which are hereby incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0004] The present invention relates generally to self-assembled semiconductor quantum dot lasers. More particularly, the present invention is directed towards quantum dot vertical cavity surface emitting lasers (QD-VCSELs).

2. Description of Background Art

[0005] Vertical cavity surface emitting lasers (VCSELs) are of interest for a variety of applications. Some of the advantages of a conventional VCSEL include

surface emission, a nearly round emission pattern, a low threshold current, and the potential for high-yield, low cost manufacturing and packaging.

[0006] FIG. 1 illustrates some of the features of a conventional VCSEL 100. A bottom mirror 105 is disposed on a substrate 102. An active region 110 is disposed between the bottom mirror 105 and a top mirror 120. A conventional VCSEL typically includes a quantum well active region for providing optical gain. A quantum well active region typically includes one or more quantum wells capable of providing a comparatively high optical gain. Optical feedback is typically provided by top and bottom distributed bragg reflector (DBR) mirror structures. In a DBR mirror VCSEL, the mirrors typically comprise pairs of alternating high index and low index semiconductor layers, with each layer typically being approximately a quarter wavelength in optical thickness. The active region is typically a high index region approximately an integer number of half wavelengths in thickness having a gain region disposed in its center.

[0007] Quantum dot (QD) VCSELs are of potential interest for a variety of applications. Each quantum dot consists of an island of low bandgap material surrounded on all sides by a higher bandgap material. The low bandgap island of each quantum dot is sufficiently small that each dimension (length, width, and height) is smaller than the thermal deBroglie wavelength over operating temperatures of interest. As a consequence, the quantum dot has its energy

states quantum confined in three dimensions, resulting in a delta-like density of states (e.g., a high density of states in a finite energy band around each permissible optical transition, analogous to a density of states for atoms).

[0008] Quantum dot active regions have a variety of characteristics that make them of interest for VCSELs, such as potential advantages in regards to temperature sensitivity and high-speed modulation. However, there are several technical barriers that have hindered the commercial exploitation of QD-VCSELs.

[0009] One barrier to the commercial exploitation of QD-VCSELs is that conventional quantum dot active regions typically have a peak optical gain that is low compared with quantum wells due to the small fill factor of quantum dots. Moreover, the optical gain at the ground state energy level saturates in quantum dots. The optical gain available from a layer of quantum dots is typically about an order of magnitude lower than that which can be achieved from a quantum well. For example, in edge-emitting lasers, the maximum ground state gain that can be achieved from a single layer of quantum dots is typically in the range of about 5 to 10 cm^{-1}.

[0010] Another barrier to the commercial use of QD-VCSELs is that many commercial applications have demanding operational requirements. For example, some applications, such as ten-gigabit Ethernet (10-GigE) require that the VCSEL operate in an uncooled transceiver over an extended temperature

range (e.g., up to about 85 °C), operate at a nominal wavelength of about 1310 nanometers (nm), and have sufficient differential gain over all operating conditions to be modulated at the desired data rate. However, since the maximum ground state optical gain decreases with increasing operating temperature this requirement further exacerbates the difficulty of designing a QD-VCSEL having sufficient optical gain to operate within ambient temperature ranges of commercial interest.

[0011] What is desired is a QD-VCSEL with improved manufacturability and desirable performance characteristics.

SUMMARY OF THE INVENTION

[0012] A quantum dot vertical cavity surface emitting laser has a low cavity loss and a correspondingly low threshold gain. To begin with, at least one of the mirrors of the laser cavity is an ultrahigh reflectivity distributed bragg reflector (DBR) mirror with mirror pairs comprised of alternating layers of high refractive index semiconductor and low refractive index oxide.

[0013] Doped intracavity contact layers between the DBR mirrors provide current to a quantum dot active region. In a preferred embodiment, the contact layers have a thickness of about a half a wavelength or less to reduce free carrier loss. In one embodiment, about a quarter of a wavelength or less of each contact

layer is heavily doped. The heavily doped portions of the contact layer may be positioned to have a low optical overlap with the longitudinal mode to reduce the free carrier loss.

[0014] In one embodiment, additional mode control layers are disposed between the DBR mirrors and the active region to reduce the optical overlap of the mode in doped regions and increase the optical confinement in the active region. In a preferred embodiment, the mode control layers are approximately quarter wavelength thick regions, have a refractive index different than adjacent layers, and are positioned to produce resonant reflections that beneficially increase the optical confinement of the longitudinal optical mode in the quantum dot active region and reduce optical confinement in heavily doped contact regions.

[0015] In one embodiment, each ultrahigh reflectivity DBR mirror is formed using a lateral oxidation process to convert oxidizable semiconductor layers into low refractive index oxides. In one embodiment, delamination of laterally oxidized mirror layers is inhibited by including intermediate composition layers to reduce residual stress. In another embodiment, one or more openings is arranged to permit lateral oxidation of bottom mirror regions while preserving lateral support regions to support the bottom mirror layers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] FIG. 1 illustrates a prior art vertical cavity surface emitting laser design.

[0017] FIGS. 2A, 2B, and 2b illustrate vertical cavity surface emitting lasers in accord with embodiments of the present invention.

[0018] FIG. 3. illustrates one embodiment of a mirror pair for a DBR mirror having laterally oxidizable layers.

[0019] FIG. 4A is a top view illustrating a VCSEL having openings formed through oxidizable bottom DBR mirror layers which have been used to laterally oxidize a bottom DBR mirror while retaining regions for laterally supporting the bottom DBR mirror of the VCSEL.

[0020] FIG. 4B is a cross sectional view through line A-A of FIG. 4A.

[0021] FIG. 4C is a cross sectional view through line B-B of FIG. 4A.

[0022] FIGS. 5A and 5B show layer sequences of VCSELs having an active region including a mode control layer with different intracavity contact layer implementations.

[0023] FIG. 6A shows a layer sequence of an embodiment having two mode control layers.

[0024] FIG. 6B illustrates in more detail an embodiment of a layer sequence for an active region and mode control layers along with illustrative thicknesses in terms of the optical wavelength in the laser.

[0025] FIG. 7 shows a sequence of epitaxially grown layers for one embodiment of a VCSEL for producing light with a wavelength around about 1300 nanometers.

[0026] FIG. 8 shows plots of the refractive index of key layers for the layer sequence VCSEL of FIG. 7 and the calculated intensity of the longitudinal mode.

[0027] FIG. 9 is a plot of quantum dot density versus growth temperature for self-assembled InAs quantum dots grown by molecular beam epitaxy on InGaAs layers.

[0028] FIG. 10 shows plots of modal gain versus current density for two different quantum dot densities.

[0029] FIG. 11 is a plot illustrating a jump in gain associated with excited states of the quantum dots at high current densities.

[0030] FIG. 12A illustrates preferred quantum dot growth parameters for InAs quantum dots and FIG. 12B illustrates a technique for embedding quantum dots in quantum wells.

[0031] FIG. 13 illustrates an embodiment in which quantum dot layers are placed proximate a single antinode.

[0032] FIG. 14 illustrates an embodiment in which quantum dot layers are placed proximate two antinodes.

[0033] FIG. 15A is a perspective view illustrating a processed VCSEL.

[0034] FIG. 15B illustrates a top mirror mesa etch mask step to etch to a first contact layer and holes for vertical isolation of the two contact layers using lateral oxidation.

[0035] FIG. 15C illustrates a first metal deposition step.

[0036] FIG. 15D illustrates an etch step to etch to a second contact layer.

[0037] FIG. 15E illustrates a second metal deposition step.

[0038] FIG. 15F illustrates a bottom mirror opening etch step.

[0039] FIG. 15 G illustrates a top view of a fabricated VCSEL.

[0040] FIG. 16A is an illustrative graph of longitudinal mode intensity in a VCSEL without mode control layers.

[0041] FIG. 16B is an illustrative graph of longitudinal mode intensity in a VCSEL having mode control layers.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0042] The present invention is directed towards quantum dot vertical cavity surface emitting lasers (QD-VCSELs) having a low cavity loss and a correspondingly low threshold gain. One application of the VCSELs of the

present invention is for high data rate communication systems with an emission wavelength greater than about 1290 nanometers (nm) in which the VCSEL must lase over an extended range of ambient temperatures (e.g., 0 °C to 85 °C). However, it will be understood that the VCSELs of the present invention may be utilized in a variety of applications.

[0043] Referring to FIGS. 2A, 2B, and 2C, a QD-VCSEL 200 of the present invention has a quantum dot active region 210 disposed between a bottom surface 204 of a top mirror 220 and a top surface 208 of a bottom mirror 205. A so-called "microcavity," a laser cavity having an extremely short effective cavity length, is formed in the region between the two mirrors 205 and 220. Each mirror 205 and 220 is a distributed bragg reflector (DBR) mirror with a $\lambda/2$ refractive index variation associated with a sequence of mirror pairs, where λ is the emission wavelength of laser light inside the laser cavity. As used hereinafter, it will be understood that layer thicknesses referred to in reference to "λ" or "wavelength" refers to a desired optical thickness with respect to the wavelength of the laser light within the laser, with the wavelength in the laser being $\lambda = \lambda_0/n_r$, where λ_0 is the free space wavelength and n_r is the effective refractive index in the laser. It will also be understood that thicknesses referred to in terms of fractions of wavelengths (e.g., $\lambda/4$, $\lambda/2$, λ) are desired nominal

target thicknesses but that some variation in actual thicknesses about the target thicknesses is consistent with the optical physics of operation.

[0044] Bottom mirror 205 is disposed on a substrate layer 202. In the processed VCSEL, each mirror has a corresponding top, bottom, and side with respect to a longitudinal optical mode reflected between the two mirrors. As described below in more detail, in a preferred embodiment at least one of the mirrors is a high reflectivity oxide/semiconductor DBR mirror formed by a lateral oxidation process.

[0045] Contact layers 240 and 230 have doped regions to permit electron-hole pairs to be injected to the active region 210 responsive to a current. Contact layers 230 and 240 are also known as "intracavity" contact layers because in the processed device they permit current to be provided from contact layers disposed within the optical cavity. A current aperture layer, (e.g., a selectively oxidizable layer that may be oxidized outside of the VCSEL to reduce deleterious currents) is preferably included as part of at least one of the contact layers. In the processed VCSEL, mesa etching may be used to expose the contact layers and suitable metal contact layers deposited to form ohmic contacts to portions of the contact layers.

[0046] VCSEL 200 is grown using a suitable epitaxial growth technique for growing self-assembled III-V semiconductor quantum dot active regions, such as

molecular beam epitaxy (MBE) or metal-organic vapor phase epitaxy (MOVPE). For a variety of commercial applications the quantum dots may be selected to have a ground state transition energy corresponding to a wavelength in the range of about 1290 nm to 1330 nm or 1480 to 1620 nm. In one embodiment the VCSEL is grown on a GaAs substrate 202 using MBE, the mirrors 205 and 220 are grown as AlGaAs layers having aluminum molar fractions selected to form mirror pairs with a $\lambda/2$ variation in refractive index (e.g., two $\lambda/4$ layers having different refractive indices) , and the quantum dot active region 210 comprises one or more quantum dot layers, with each layer of quantum dots being a layer of self-assembled InAs quantum dots embedded in an InGaAs quantum well having GaAs quantum well barriers. More generally, however, active regions utilizing InAs quantum dots may be grown to have ground state emission wavelengths over a range of wavelengths.

[0047] In a quantum dot laser, each layer of quantum dots has only a limited maximum gain at the ground state transition energy due to the delta-like density of states function of quantum dots. For self-assembled quantum dots there is also typically a limit on the number of quantum dot layers that can be employed without generating deleterious strain. As a further consideration, the optical gain decreases with increasing active region temperature. Thus, to achieve ground state operation over an extended range of operating temperatures it is

necessary to design the VCSEL to have an extremely low threshold gain required for lasing.

[0048] The saturated ground state gain depends upon several parameters. Studies by the inventors indicate that a saturated ground state gain of as high as 25 cm^{-1} may be achieved using a quantum dot active region having several InAs quantum dot layers. Thus, it is desirable to have a VCSEL with a threshold gain below about 25 cm^{-1}.

[0049] The threshold lasing condition for a quantum dot VCSEL similar to that shown in FIG. 2 is given by:

$$\Gamma_{qd} g_{qd} = \Gamma_c \alpha_c + \frac{1}{L_{eff}} \log\left(\frac{1}{R_{eff}}\right) \quad \text{Eq. 1A}$$

Where Γ_{qd} is the optical confinement of the quantum dot layers, g_{qd} is the gain of a quantum dot layer, Γ_c is the optical confinement in the contact layers, α_c is the free carrier loss associated with doping the contact layers, L_{eff} is the effective cavity length of a longitudinal mode reflected between the two mirrors, and R_{eff} is the effective mirror reflectivity associated with the top and bottom mirror layers and is conventionally the product of the top and bottom mirror reflectivities. The term $\frac{1}{L_{eff}} \log\left(\frac{1}{R_{eff}}\right)$ is also commonly known as the "mirror loss." The mirror reflectivity, active layer thickness, and contact layer

thicknesses will also affect the optical confinement of the quantum dot layers and the optical confinement in contact layers.

[0050] The ground state transition energy has a saturable gain that is temperature dependent. The saturated gain must be greater than the threshold gain for lasing to occur at the ground state energy level. Thus, Eq. 1 can be rewritten as:

$$\Gamma_{qd} g_{qd-sat} > \Gamma_c \alpha_c + \frac{1}{L_{eff}} \log\left(\frac{1}{R_{eff}}\right) \quad \text{Eq. 1B}$$

where g_{qd-sat} is the saturated gain.

[0051] It can be understood from Eq. 1B that the operable temperature range of a QD-VCSEL is improved by designing a vertical optical structure that simultaneously has a high effective mirror reflectivity, a comparatively high quantum dot confinement factor, and a comparatively low optical confinement in lossy contact regions. Note that for the case of extremely high reflectivity mirrors that the free carrier loss will dominate in Eq. 1B. For the case of ultra high reflectivity mirrors, then, the expression may be approximated as:

$$\Gamma_{qd} g_{qd-sat} > \Gamma_c \alpha_c \quad \text{Eq. 1C}$$

[0052] Low Mirror Loss Design

The magnitude of the reflectivity, R, of a DBR mirror is commonly approximated by:

R=kNΔn/n, where N is the number of mirror pairs, n is the average index of refraction of the two layers, k is a constant (or a function of Δn/n), and Δn is the difference in index of refraction for the two layers. For a semiconductor/semiconductor mirror the refractive index is typically small, such that a large number of mirror pairs are required to achieve a high DBR mirror reflectivity. For example, in the GaAlAs system a GaAs/AlAs mirror pair has a refractive index step of only about 0.6. Consequently, to form an ultra high reflectivity DBR mirror (e.g., a mirror reflectivity of greater than 99.99%) would require growing a large number of mirror pairs, which would result in extremely thick DBR mirrors that would be impractical to grow and process.

[0053] The effective reflectivity of the mirrors 205 and 220 is increased if at least one of the mirrors in the processed VCSEL has oxide/semiconductor mirror pairs with a high index step between adjacent mirror layers of each mirror pairs. In accord with one embodiment of the present invention, the epitaxially grown layers of at least one of the mirrors 205 or 220 is grown to have a sequence of mirrors pairs of oxidizable semiconductor layers and substantially nonoxidzable semiconductor layers. The oxidizable semiconductor layer is laterally oxidized in a post-growth process to convert it into a metal oxide having a substantially lower refractive index than the as-grown layer. In the III-V compound semiconductor material system, the oxidation rate increases with increasing

aluminum molar fraction. For example, when an AlGaAs layer with an aluminum molar fraction greater than about 0.90 is exposed to steam and nitrogen at a temperature of about 450 °C, the arsenic is converted to arsine leaving behind an amorphous mixture of aluminum oxides, gallium oxides, and residual hydrogen. The rate of oxidation is highly dependent upon the aluminum molar fraction, with AlAs oxidizing extremely rapidly. $Al_{0.98}Ga_{0.02}As$ oxidizes about three times faster than $Al_{0.96}Ga_{0.04}As$ and ten times faster than $Al_{0.92}Ga_{0.08}As$.

[0054] Metal oxides typically have a low refractive index compared with III-V semiconductors. This permits a post-growth oxidation step to be used to create a DBR mirror having a sequence of oxide and semiconductor layers such that a large refractive index step between mirror pair layers may be achieved, permitting a high DBR mirror reflectivity to be achieved. For example, the as-grown DBR mirror may comprise a sequence of pairs of high/low aluminum composition AlGaAs layers, such as AlAs/AlGaAs or AlAs/GaAs layers. For this case, the refractive index step is increased to about 2.0 by selectively oxidizing the AlAs layer into AlO_x (refractive index of about 1.6) in a post-growth oxidation process. The corresponding reflectivity for a 1.3 micron wavelength emission laser is calculated to be 99.9341% for five DBR mirror pairs and 99.99922% for eight mirror pairs.

[0055] As indicated in FIG. 2A, the top-mirror 220 may comprise an oxide/semiconductor DBR mirror whereas the bottom mirror 205 comprises a semiconductor DBR mirror. Alternatively, the bottom mirror 205 may comprise an oxide/semiconductor DBR mirror while the top mirror 220 comprises a semiconductor DBR mirror. Referring to FIG. 2C, it will also be understood that both the top and bottom mirrors 205 and 220 may comprise oxide/semiconductor mirrors.

[0056] Oxide/semiconductor DBR mirrors formed by laterally oxidizing high Al composition layers have a tendency to delaminate, particularly if large unsupported areas are completely oxidized. One factor likely to cause delamination is the residual strain at the interface between the oxidized layer and the unoxidized semiconductor. Consequently, in one embodiment of the present invention the semiconductor mirror structure and mirror oxidation process is selected to inhibit mirror delamination during processing and subsequent operation of the VCSEL.

[0057] FIG. 3 is a diagram illustrating a sequence of grown DBR mirror pair layers (prior to lateral oxidation). In one embodiment, an oxidizable semiconductor layer 305 is connected to a substantially non-oxidizable semiconductor layer 315 by an intermediate layer 310. The composition of the oxidizable semiconductor layer is preferably selected to have a controllable

oxidation rate in a lateral oxidation process. Intermediate layer 310 preferably has a composition selected to inhibit delamination of layer 305 from layer 315. The relative thickness of layers 305, 310, and 315 are selected to form DBR mirror pairs with subsequent lateral oxidation of the oxidizable layers.

[0058] In one embodiment, the non-oxidizable semiconductor layer 315 comprises a layer of AlGaAs having a first molar fraction of aluminum while the oxidizable layer 305 comprises a layer of AlGaAs having a second, higher molar fraction of aluminum. AlAs oxidizes extremely rapidly. AlGaAs with an aluminum molar fraction below about 0.95 oxidizes comparatively slowly. Consequently, in one embodiment the oxidizable layer has an aluminum molar fraction of between about 0.97 to 0.99, with 0.98 being preferred. For this case, intermediate layer 310 may comprise a region in which the aluminum molar fraction is graded between the aluminum composition of layers 305 and 315 (e.g., $Al_{0.92}Ga_{0.08}As$). The intermediate layer improves adhesion and is believed to reduce mechanical instabilities associated with residual strain at the interfaces.

[0059] In a lateral oxidation process, side portions of the mirror layers must be exposed for oxidation. For a lateral oxidation process for a top mirror, the same mesa etch used to form the top mirror mesa is sufficient to expose side portions of mirror layers for oxidation. However, lateral oxidation of bottom mirror layers is more difficult. A laterally oxidized bottom DBR mirror tends to

have significant residual strain energy due to the fact that it may be larger in area than the top mirror and because the bottom mirror, which supports other portions of the VCSEL, cannot relieve strain from exposed surfaces as readily as the top mirror. Thus, a laterally oxidized bottom DBR mirror is of particular concern in regards to delamination.

[0060] In one embodiment of a bottom DBR mirror oxidation process, the lateral oxidation process is performed through one or more openings (e.g., etched trenches) formed in the bottom mirror layers. As illustrated in the top view of FIG. 4A, the openings 410 are spaced far enough apart that the VCSEL's bottom DBR mirror 420 is laterally supported. The oxidation conditions are adjusted such that the lateral oxidation 440 spreads throughout the desired bottom DBR mirror region. The spacing between the openings 410 and their location relative to the intended lasing region of the bottom mirror may be selected to retain connection portions 430 of the DBR mirror layers that connect the oxidized DBR mirror to unoxidized mirror layers 450.

[0061] Referring to FIG. 4A, in one embodiment of the present invention a process for laterally oxidizing a bottom mirror includes opening oxidation windows 410 proximate a side portion of the VCSEL's bottom DBR mirror 420. As one example, one or more trench openings may be formed that expose a portion of at least one side of oxidizable DBR mirror layers for the bottom DBR

mirror. For example, two parallel trenches may be formed near the sides of the bottom VCSEL mirror 420. During the oxidation process, the oxidizable mirror layers are oxidized laterally about the openings 410. The composition of the oxidixable layer and the oxidation conditions (e.g., nitrogen/steam temperature and time) are selected such that the oxidizable layers in the bottom DBR mirror are oxidized substantially throughout the area 420 of the bottom mirror of the VCSEL which will reflect laser light.

[0062] FIG. 4B is a cross sectional view through line A-A of FIG. 4A. Proximate trenches 410 the bottom mirror 205 is laterally oxidized. In a VCSEL process, a top mirror 220 may be defined by a mesa etch and suitable p contact 490 and n-contact layers 480 deposited on the contact layers 230 and 240. In one embodiment, top mirror 220 is laterally oxidized in the same oxidation step. Additionally, a current aperture layer 495 may also be oxidixed to limit current flow to VCSEL lasing regions.

[0063] FIG. 4C is a cross-sectional view through line B-B of FIG. 4A. Note that lateral support to the bottom DBR mirror layer is provided in regions where the oxidized bottom mirror (outside of the VCSEL) is connected to unoxidized mirror material, thereby supporting the oxidized mirror and inhibiting delamination. Referring to FIG. 4A, it will be understood that it is desirable to select process conditions that oxidize the bottom DBR mirror in VSCEL areas that

will emit light while also minimizing the total oxidized area 440 consistent with oxidizing bottom VCSEL mirror 420.

[0064] Contact Layer Design

In a VCSEL with at least one ultrahigh reflectivity oxide/semiconductor DBR mirror, the longitudinal optical mode will be tightly confined between the DBR mirrors 205 and 220. The contact layers 230 and 240 require a sufficient doping-thickness product to achieve an acceptable ohmic resistance. However, if the contact layers 230 and 240 are heavily doped, this can result in substantial optical losses due to free-carrier losses in the contact layers unless the thickness and doping profile of the contact layers is appropriately selected. Consequently, in one embodiment of the present invention the contact layers have a thickness and doping profile selected to permit a reasonable ohmic resistance to be achieved with a comparatively low optical loss.

The electrical contact layers 230 and 240 are designed to provide electron hole pairs into the quantum dot active region layers. The contact layers form a p-n diode junction for injecting electron hole pairs into quantum dot active region 210. For example, contact layer 240 may include a heavily doped p-type layer whereas contact layer 230 may include a heavily doped n-type layer. Additional current aperture layers (not shown in FIGS. 2A-2C) are preferably

included to limit current injection to intended laser regions. In particular, the current aperture layers may comprise a layer of AlGaAs that is also oxidized in regions disposed away from the active region of the VCSEL, such as under contact pad metallizations. In one embodiment, the contact layers and associated aperture layers have a thickness of about a half of a wavelength. In one embodiment, the contact layers are not uniformly doped but instead are doped most heavily in regions where the optical field has the lowest intensity in the contact layers.

[0065] Doped contact layers 230 and 240 have an optical loss associated with free carrier absorption. The free carrier absorption increases with dopant concentration and the magnitude of the electric field of the longitudinal optical mode. The optical mode intensity outside of the active region 210 between DBR mirrors approximates an envelope function within which the intensity varies with a periodicity determined by the wavelength. Selecting each contact layer to have an optical thickness of less than about $\lambda/2$ facilitates placing the peak doping proximate an optical node of the longitudinal mode (e.g., a region having a low intensity). The precise free carrier loss may be minimized by using a computer analysis technique to integrate the loss through the contact layer based upon the dopant concentration and field strength at each point within the contact layer.

[0066] In one embodiment, each contact layer has a thickness of about $\lambda/2$ or less and includes a heavily doped layer having a thickness of about $\lambda/4$ or less. Selecting the heavily doped portion of the contact layers 230 and 240 to have a thickness of about $\lambda/4$ facilitates reducing the optical losses because the most heavily doped portion may be placed proximate a node in the optical intensity, e.g., the overlap of the field intensity is reduced. Consequently, in a preferred embodiment of the present invention the thickness of the contact layers is selected to be about $\lambda/2$ or less. In one embodiment, heavily doped contact layers have a thickness of about $\lambda/4$ or less.

[0067] The optical absorption of the contact layers may also be reduced by grading the doping concentration to have a higher doping concentration in regions where the longitudinal mode has a lower intensity. Referring to FIGS. 5A and 5B, for p-contact layers in the GaAs materials system the p-contact layers 240 may comprise a highly doped p-type GaAs layer 505 proximate the bottom 204 of the top DBR mirror 220 and having a thickness of about $\lambda/4$. The remaining $\lambda/4$ thickness closest to the active region comprises a p-type GaAs layer 510 and AlGaAs current aperture layer 515 (e.g., a layer that can be selectively oxidized in contact pad regions to reduce parasitic conduction). A suitable n-type contact layer 230 may comprise a heavily n-doped GaAs layer 540

proximate the top surface of the bottom DBR mirror 205 and an AlGaAs current aperture layer 545.

[0068] An additional benefit of reducing the thickness of the contact layer thickness to an optical thickness of about $\lambda/2$ or less is that it increases the relative fraction of the mode confined to the active region. In particular, in a VCSEL with ultrahigh reflectivity mirrors only a small fraction of the light resides in the mirror layers. Following the procedures described in the present patent application, a reduction in the confinement factor of the mode in the contact layers results in a corresponding increase in the optical confinement factor within the active region.

[0069] Mode Control Layer to Reduce Contact Layer Absorption

Referring to FIGS. 5A and 5B, in one embodiment of the present invention the active region has an at least one associated mode control layer to further reduce optical loss in the contact layers. The function of the mode control layer is to adjust the shape of the longitudinal mode to beneficially reduce Γ_c and achieve a high Γ_{qd}. One example of a mode control layer is any layer having a refractive index profile that adjusts the optical mode to place a longitudinal node proximate heavily doped contact layers such as to reduce the free carrier loss associated with the contact layers.

[0070] In one embodiment, the mode control layers create reflections selected to produce a resonance effect that beneficially alters the longitudinal mode intensity distribution between the top and bottom mirrors 205 and 220. As one example, each mode control layer may comprise a single layer functioning as a mirror layer and permitting the passage of an electrical current, with the mirror layer reducing the optical intensity within the contact layers. As indicated in FIG. 5B, in one embodiment the active region is an integral number of half-wavelengths in thickness and includes a plurality of quantum dot layers, with each quantum dot layer being a plurality of quantum dots embedded in a quantum well. It should be understood that other VCSEL designs could result in the presence of quarter-wave phase shift layer with concomitant change in the other layer thicknesses. In this embodiment, the mode control layers comprise an approximately quarter wavelength thickness region of low index or high index layers.

[0071] Referring to FIG. 6A, in one embodiment, each of the mode control layers 610 are regions disposed between the first or second ends 602 or 604 of the active region 210 and a respective mirror. In one embodiment, each mode control layer is a $\lambda/4$ thick layer having a different refractive index than adjacent layers (e.g., functions a partial DBR mirror). The difference in refractive indices between the mode control layer 610 and adjacent layers creates optical

reflections. By appropriately selecting the thickness of the active layer, contact layers, and mode control layers, a resonance condition is established with the additional reflections of the mode control layers 610 beneficially altering the longitudinal mode intensity profile between the mirrors.

[0072] A detail of an exemplary active region with mode control layers 610 are shown in FIG. 6B. Active region 210 includes quantum dot layers 655 with InAs quantum dots 690. The mode control layers 610 may comprise layers having either a lower or higher refractive index than adjacent layers. If the refractive index is higher, the thickness of the active region is preferably an integer number of half wavelengths. If the refractive index is lower, than the active region is preferably an odd multiple of quarter wavelengths in thickness. and GaAs barrier layers 660.

[0073] The resonant reflections can be used to create large changes in longitudinal mode intensity between top and bottom DBR mirrors. FIG. 16A illustrates optical field intensity 1600 versus distance across the active and contact layers of a VCSEL having high reflectivity top and bottom DBR mirrors in a structure that does not have mode control layers 1610. For the purposes of illustration, VCSEL cavity components are superimposed on the plot. For typical contact layer alloy compositions and active layer structures the refractive indices of the layers is approximately uniform over optical-scale distances.

Consequently, the longitudinal optical mode is essentially periodic between the two mirrors. This results in a high overlap of the field in contact layers, resulting in high cavity losses.

[0074] FIG. 16B is a plot 1650 of longitudinal mode intensity versus distance in a VCSEL that illustrates the effect of mode control layers 610 having a refractive index profile and placement selected to produce a resonance condition. In this example, the mode control layers are quarter wavelength thick mode control layers comprised of a lower index material (e.g., AlGaAs layers). The resonant reflections from the mode control layers simultaneously increases the optical confinement factor of the active region while also reducing the confinement of the mode in the contact layers. The result for a VCSEL with optimized contact layer thicknesses is that the optical confinement factor, Γ_{qd}, of quantum dot layers in the active region increases by a factor of about two and the contact layer confinement factor, Γ_c, simultaneously decreases by about a factor of two. The net result is that the threshold gain decreases by up to a factor of four.

[0075] FIG. 7 shows an exemplary sequence of grown layers for a quantum dot VCSEL 700 including DBR mode control layers. Exemplary thicknesses, dopings, and MBE growth temperatures are shown. FIG. 8 shows plots of mode intensityy 810 and refractive indices 820 through the VCSEL (with oxidized

AlAs mirror layers). The active region includes three InGaAs quantum wells approximately 9 nm in thickness. Approximately 2.4 monolayers of indium are deposited under growth conditions selected to form quantum dots, e.g., 1 nm of the quantum well is grown, approximately 2.4 equivalent monolayers of Indium Arsenide are deposited to form InAs islands, and a top 8 nm InGaAs layer is deposited to embed the InAs islands. In this example, the mode control layers 610 comprise 107 nm thick regions of $Al_{0.92}Ga_{0.08}As$. The top and bottom DBR mirrors 205 and 220 comprise alternating nominally AlAs/GaAs layers. For improved processing control, the AlAs layer is preferably $Al_{0.98}Ga_{0.02}As$, since this facilitates controlling the rate of lateral oxidation. Between each pair of AlAs/GaAs layers is an intermediate layer of $Al_{0.92}Ga_{0.08}As$ to inhibit delamination. The contact layers are preferably doped to reduce ohmic contact resistance. Layers which are to be oxidized are preferably lightly doped or undoped. Electrical interfaces between regions having different AlGaAs compositions may be graded in composition, if desired, to reduce electrical resistance. Note that the number of mirror pairs of each mirror does not have to be identical, e.g., in this example the bottom mirror 205 has more mirror pairs than the top mirror 220. Additionally, it can be seen in FIGS. 7 and 8 that a mode control layer 610 may be placed between one or more of the contact layers. In particular, in some applications it is desirable to place a current aperture layer as

close to the active regions as possible, in which case the mode control layer may be placed between the current aperture layer and highly doped contact layers.

[0076] Referring to FIG. 8, the longitudinal mode intensity 810 is tightly confined about the active region with an antinode centered in the quantum dot layers. The longitudinal mode has an antinode proximate each contact layer, which reduces optical absorption. The doping within each contact layer may also be graded to have a peak doping concentration in regions having a low optical intensity, thereby further reducing optical absorption.

[0077] Active Layer Design for Increased Gain

The modal quantum dot gain may be increased by selecting growth parameters that increase the quantum dot density, increasing the number of quantum dot layers consistent with strain limitations, and arranging the quantum dot layers to increase the optical confinement factor of the quantum dots.

[0078] A preferred growth technique is molecular beam epitaxy (MBE) with the quantum dot layer grown at a temperature between about 450 °C to 540 °C. The other layers (top mirror, bottom mirror, and contact layers) are preferably grown at a temperature below about 600 °C (e.g., 580°C to 600 °C) to limit the possibility of blue-shifting of the quantum dots as a result of diffusion of quantum dot layers. A conventional optical pyrometer may be used to

determine the temperature. The arsenic flux is preferably chosen to achieve an arsenic stabilized surface.

[0079] In a preferred embodiment, the quantum dots form as self-assembled islands. InAs has a relaxed lattice constant that is more than about 2% greater than the underlying semiconductor layers, a Stranski-Krastanow (S-K) growth mode occurs once a sufficient number of equivalent monolayers of InAs are deposited. In the S-K growth mode, the driving force for the formation of islands is the reduction in strain energy afforded by elastic deformation, i.e., for S-K growth it is more energetically favorable to increase surface energy by islanding than by relaxing strain by dislocation generation. In a S-K growth mode, the growth becomes three dimensional after a critical thickness of the larger lattice constant material is grown upon an initial wetting layer.

[0080] FIG. 9 is a plot of quantum dot density versus MBE growth temperature for quantum dots grown on two different InGaAs well layer compositions. It can be seen that the dot density depends strongly upon temperature and also upon the composition of the bottom well layer. Dot densities of greater than 1×10^{11} cm^{-2} may be achieved at a growth temperature of about 470 °C. The dot density can be adjusted by more than a factor of five by selecting a growth temperature between 470 °C to 540 °C. Experiments indicate that the dot density is at least a factor of two higher when the dots are grown on

an InGaAs layer compared with a GaAs layer at a comparable temperature. The dot density also increases when the InGaAs alloy composition is increased from $In_{0.1}Ga_{0.9}As$ to $In_{0.2}Ga_{0.8}As$. Experiments by the inventors indicate that the thickness of the bottom InGaAs well layer may be extremely thin and still have the same effect as a thick layer in regards to the nucleation of quantum dots on the bottom InGaAs layer. Thus, to achieve a reproducible dot density, the bottom well layer need only have a thickness consistent with it having a reproducible thickness and alloy composition. The bottom well layer may have a thickness as low as 0.5 nm, although a thickness of about one nanometer may be easier to reproducibly grow.

[0081] FIG. 10 is a plot of modal gain versus current density of edge emitting lasers for two different dot densities. It can be seen in FIG. 10 that the modal gain of each quantum dot layer increases with increasing dot density. Consequently, in one embodiment a quantum dot growth temperature is selected to increase the quantum dot density. The ground state gain of a quantum dot has a maximum (saturated) optical gain due to the delta-like density of states of quantum dots. However, at high pumping levels additional excited states may be accessible to provide additional gain at shorter wavelength, as indicated in the plot of FIG. 11.

[0082] FIGS. 12A and 12B shows exemplary growth temperatures and thicknesses for a quantum dot layer. FIG. 12A shows embedded quantum dots (QDs) and FIG. 12B shows a corresponding growth layer sequence. The quantum dots 1210 are formed on a first well layer 1205 of InGaAs and embedded in a second well layer 1215 of InGaAs. In one embodiment, a bottom InGaAs quantum well layer of between about 0.5 to 2 nm in thickness is grown on top of a GaAs barrier layer. An InAs floating layer is preferably initially deposited on the GaAs layer to raise the surface indium concentration close to its equilibrium concentration at the growth temperature, thereby improving the compositional uniformity of subsequent InGaAs layers. The equilibrium concentration of segregated (floating) indium depends on temperature and InGasAs composition but is typically about 0.5 to 1 monolayers over a range of common growth parameters.

[0083] An InGaAs quantum well composition of between about $In_{0.1}Ga_{0.9}As$ to about $In_{0.2}Ga_{0.8}As$ is preferred. Higher indium molar fractions tend to increase the dot density and the depth of the energy barrier for confining electrons and holes in the quantum well. However, higher indium concentrations also increase the strain associated with each layer. Typically about 1 to 3 monolayers of InAs is deposited to form InAs islands. A top well layer of about 6 to 11 nanometers of InGaAs may be used to embed the InAs. A GaAs layer of about 10-40 nm is

grown to form a second quantum well barrier. In one embodiment, a desorption step is performed after growth of the top InGaAs layer to planarize any residual InAs islands that protrude above the top InGaAs layer. The time and temperature of the desorption step are preferably selected to rapidly planarize protruding InAs regions but to preserve InGaAs. In one embodiment, several monolayers of GaAs are deposited before the desorption step to facilitate maintaining a stable top InGaAs well layer during the desorption step.

[0084] The number of quantum dot layers and their spacing is limited, in part, by strain effects. The strain thickness product of an individual layer of quantum dots should be sufficiently low to prevent the formation of deleterious dislocation and defects. Additionally, the cumulative strain associated with all of the layers should be sufficiently low to prevent the formatting of deleterious defects. For a sequence of quantum dot layers of an active region 210, an average strain-thickness product should be below a threshold average strain (e.g., 0.5%). The strain thickness product of an individual quantum dot layer is E_wT_w, where E_w is the strain of a well layer and T_w is the thickness of the well. The strain thickness product of an individual barrier layer is E_bT_b, where E_b is the strain of the barrier layer and T_b is the thickness of the barrier layer. For a sequence of n layers of dots, the average strain, E_{av}, is:

[0085] $E_{av}= \frac{(n+1)EbTb + nEwTw}{(n+1)Tb + nTw}$ Eq. 2.

[0086] For GaAs barriers (which are unstrained), this simplifies to:

[0087] $E_{av}= \frac{nEwTw}{(n+1)Tb + nTw}$ Eq. 3.

[0088] Equation 2 can be re-expressed as a relationship between the barrier thickness, well thickness, modified average strain, strain in the barriers, and strain in the well:

[0089] $Tb=\frac{nTw(Ew-Eav)}{(n+1)(Eav-Eb)}$ Eq. 4

[0090] For GaAs or AlGaAs layers grown on a GaAs substrate $E_b \approx 0$ so that the barrier thickness is:

[0091] $Tb=\frac{nTw(Ew-Eav)}{(n+1)Eav}$ Eq. 5.

[0092] Equation 5 can be used to derive a relationship for a minimum barrier layer thickness. If the average strain is selected to be less than a maximum average strain (for example, and average strain less than about 0.51%), E_{avmax}, then the following relationship holds:

[0093] $Tb>\frac{Tw[n(Ew-Eav\max)]}{(n+1)Eav\max}$ Eq.6.

[0094] As an illustrative example, if E_{avmax} is 0.4 and E_w =1.45 for an average In alloy composition of about $In_{0.2}Ga_{0.8}As$ then Tb>2.625Tw(n/(n+1)). If Tw is 9 nm

for a structure, then the minimum barrier thickness for a structure with 6 quantum dot layers is about 20 nanometers.

[0095] The quantum dot layers within the active region are preferably placed proximate an anti-node (a region of peak optical intensity) of the longitudinal mode, since this beneficially increases the optical confinement in each quantum dot layer. In one embodiment, approximately three-to-six quantum dot layers are placed about each antinode. Using less than three quantum dot layers per antinode typically produces less gain than desired for many applications. With more than six quantum dot layers per antinode, the total spacing required to be within acceptable strain limits makes it difficult to achieve a high optical confinement for each quantum dot layer. For many applications, a preferred number of quantum dot layers per antinode is three-to-four, since using more quantum dot layers tends to increase the threshold current.

[0096] In one embodiment, the active region has a thickness selected to generate a single antinode centered within the active region and mode control layers. As indicated in FIG. 13, in one embodiment, the quantum dot layers 1310 are positioned proximate the single antinode 1310 of the longitudinal mode. In an alternate embodiment, the active region and mode control layers are centered on a node and has a thickness selected such that there are at least two antinodes within the active region. In this embodiment, quantum dot layers are disposed

proximate each antinode. FIG. 14 illustrates a VCSEL having two sets of quantum dot layers 1420 with each set centered about one of two antinodes 1410. For example, each set of of quantum dot layers 1420 may comprise three or four quantum dot layers.

[0097] Device Processing

FIG. 15A is a perspective view of an exemplary processed VCSEL 1500 fabricated in accord with one embodiment of the present invention. The processing includes steps for etching down to the p-type contact layers 240 in regions outside of the desired top mirror 220 of the VCSEL. Conventional photolithography processes are used. An exemplary top mirror area is about 14 to 30 microns square. A suitable mask layer (e.g., a photoresist mask) having a mask region 1550 for protecting the top mirror during the first etch process is illustrated in FIG. 15B. The etch process may use any suitable wet or dry etch process. In one embodiment, an inductively coupled plasma (ICP) etch process is used. ICP provides the benefits of a high aspect ratio and comparatively low ion energies. After the p-type contact layer etch, a p-metal layer 1510 is deposited to form the p-contact.

[0098] FIG. 15 C shows an exemplary p-metallization. Examples of p-metal layers include Au/Zn/Au metallization. A ring 1552 of p-contact metal is formed on the p-contact layer around the top mirror mesa to provide a low electrical

resistance. In one embodiment, the ring 1552 is about ten microns wide and connected to a pad 1556 by a neck 1554 about ten microns wide and about forty microns long. An exemplary p-contact pad is about 100 microns by 100 microns in area. The p-contact layer includes holes 1558 on a pad region to permit via holes to be etched down to a current aperture layer, which is oxidized during the mirror oxidation process. As one example, each hole 1558 may be about ten microns square.

[0099] A cavity mesa etch is used to etch down to the n-type contact layer 230. A suitable mask layer is shown in FIG. 15D to protect the top mirror mesa and p-contact metallization.

[00100] A n-metal contact layer 1520 is deposited on the n-contact layer. As one example, the n-metal contact layer be a AuGe/Ni/Au contact. A suitable mask is shown in FIG. 15E. For embodiment in which there the bottom mirror layer is to be oxidized, two trenches 1570 are included. In one embodiment, each trench may be about seven microns wide and about seventy microns long. An oxygen plasma or other cleaning step may be used to clean the sample prior to lateral oxidation in a water vapor oxidation process. As indicated in FIG. 15 F, an additional mask may be used to etch a trench down through the bottom mirror. A single lateral oxidation step may be used to simultaneously oxidize the top mirror, contact pad isolation, and the bottom mirror.

[00101] FIG. 15 G shows a top view of a completed VCSEL.

[00102] Low Threshold Gain VCSELs For Extended Temperature Range Operation

An important benefit of the VCSEL structure of the present invention is that the threshold gain may be selected to be below the saturated ground state gain over an extended temperature range. As previously described, the ground state transition energy of a layer of quantum dots has a maximum gain at which the gain saturates. The saturated ground state gain decreases with increasing temperature. Thus, reducing the threshold gain increases the ambient temperature operating range, e.g., a low threshold gain permits a VCSEL to be operated at higher temperatures.

[00103] The combination of features of the present invention permits an approximately order of magnitude reduction in threshold gain compared with a conventional quantum well VCSEL. First, optical absorption in contact layers is reduced due to the comparatively thin doped contact layers (e.g., contact layers with heavily doped regions less than $\lambda/2$ in thickness), the mode control layers which reduce the optical intensity in contact layers, and the grading of doping profiles in contact layers, which places the highest doping concentrations in regions with the lowest optical intensity. Consequently, the optical absorption

in the contact layers by at least a factor of two compared with conventional VCSELs having λ thick layers.

[00104] Second, the anti-delamination features of the present invention facilitates the use of ultra-high reflectivity DBR mirrors, which also reduces the threshold gain. In particular, the anti-delamination features of the present invention permit oxide/semiconductor DBR mirrors to be manufactured that have about a factor of ten lower mirror loss than conventional semiconductor DBR mirrors. Third, the arrangement of quantum dot layers within the active region facilitates achieving a high optical confinement factor of quantum dot layers, further reducing the threshold gain requirements.

[00105] The high reflectivity mirrors in combination with the mode control layers results in an increase in the available optical gain by about a factor of 1.5 to 2 due to the increased optical confinement factor for the quantum dots. This, in combination with the approximately factor of two reduction in the optical loss in the contact layers results in the VCSEL having an approximately 3-to-4 fold improvement in gain versus loss. As an illustrative example, a typical ground-state saturated gain of a multiple layer quantum dot active layer may be 25 cm^{-1} or more at room temperature. In a VCSEL of the present invention having top and bottom oxidized mirrors, mode control layers, and thin contact layers, the cavity loss is only about 10 cm^{-1}. This means that there is a 15 cm^{-1} margin. This

permits, for example, the laser to be operated at an elevated temperature for which the saturated gain decreases by more than a factor of two (e.g., to 12.5 cm^{-1}).

[00106] Referring to FIG. 8, in one embodiment the reflectivity of top and bottom oxidized mirrors exceeds 99.9%. For example, an oxidized DBR mirror with eight AlO/GaAs DBR mirror pairs has a calculated longitudinal mode reflectivity of 99.999943% while an AlO/GaAs DBR mirror with five mirror pairs has a calculated longitudinal mode reflectivity of 99.97%. An optimized VCSEL structure similar to that shown in FIG. 8 has a quantum dot optical confinement factor of between about 1-2%, depending upon the number of quantum dot layers. The optical losses associated with contact layers has been reduced to a value about the same as the loss due to the mirror transmission. The calculated differential efficiency is about 50%.

[00107] As a consequence of the above described features, QD-VCSELS lasing in the ground state transition energy over an extended temperature range may be designed. For a particular application, such as a laser operating between a first temperature (e.g., 0°C) to a second temperature (e.g., 85 °C), the saturated ground state gain at each temperature may be calculated and the cavity loss is selected to permit lasing over the temperature range.

[00108] An edge-emitting quantum dot laser may be used to empirically determine the range of QD gain between two temperatures. The effects of the DBR mirrors may be simulated by using an external cavity laser configuration in which a diffraction grating mirror provides wavelength selective feedback to a Fabry-Perot laser ("gain chip"). The threshold gain/cavity losses for the external cavity may be determined by characterizing the external grating mirror reflectivity and coupling optics. This threshold gain is the value that the gain chip must satisfy. At the selected wavelength and its associated threshold gain, the maximum operating temperature of the laser chip can be assessed by varying its temperature alone. Thus, the relationship between gain and temperature can be incorporated into the design of the VCSEL cavity.

[00109] The VCSEL design may then be adjusted to achieve a threshold gain less than the saturated quantum dot gain at the highest operating temperature. For example, if an extended operating temperature range is desired, the mirror loss may be reduced by increasing the number of DBR mirror layers and/or using oxidized mirrors in both the top and bottom DBR mirror. Alternatively, the number of quantum dot layers may be increased.

[00110] It will be understood that the present invention is not limited to AlGaAs materials. Examples of other III-V materials systems include AlGaInAs and related ternary alloys; AlInAs and GaInAs on InP substrates; and AlGaAsSb

and AlAsSb, and GaAsSb and associated ternary alloys on InP. For example, mode control layers generating resonant reflections may be incorporated in VCSELs fabricated from a variety of materials. Additionally, since lateral oxidation occurs in a variety of III-V materials, such as alloys formed from digital alloys having AlAs layers, the lateral oxidation of bottom DBR mirrors through trench openings may be applied to a variety of III-V materials.

[00111] While particular embodiments and applications of the present invention have been illustrated and described, it is to be understood that the invention is not limited to the precise construction and components disclosed herein and that various modifications, changes and variations which will be apparent to those skilled in the art may be made in the arrangement, operation and details of the method and apparatus of the present invention disclosed herein without departing from the spirit and scope of the invention as defined in the appended claims.